

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. RA043D2DC	SERIAL NUMBER 09/545,648
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 10, 2000	GROUP ART UNIT 2181

INFORMATION DISCLOSURE
STATEMENT
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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
DA	4,633,735	05/05/87	Novak, et. al	—	—	
DA	5,684,753	11/04/97	Hashimoto, et al	—	—	
DA	4,322,635	03/30/80	Redwine	—	—	
DA	4,916,670	04/10/90	Suzuki et al.	—	—	
DA	5,006,982	04/09/91	Ebersole et al.	—	—	
DA	4,636,986	01/13/87	Pinkham	—	—	

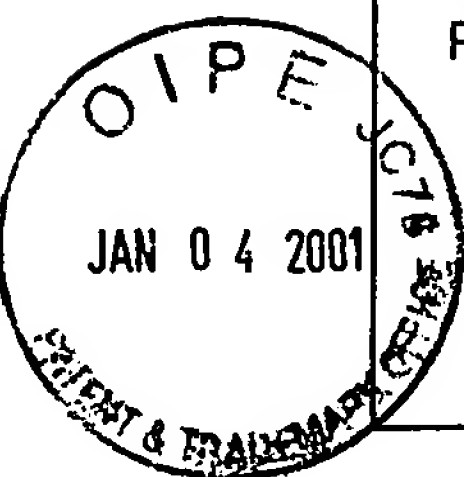
FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

DA	Ikeda, Hiroaki et al., "100 MHz Serial Access Architecture for 4MB Field Memory," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990)
DA	Takasugi, A. et al., "A DATA TRANSFER ARCHITECTURE FOR FAST MULTI-BIT SERIAL ACCESS MODE DRAM", 11TH European Solid State Circuits Conference, Toulouse France pp. 161-165 (Sep. 1985)
DA	Ray Pinkham et al., "A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988)
DA	Graham, Andy et al., "Pipelined static RAM endows cache memories with 1-ns speed", Electronic Design pp. 157-170 (Dec. 1984)
DA	Robert J. Lodi et al., "Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit," IEEE International Solid-State Circuits Conference, (Feb. 1976)
DA	Pinkham, Raymond, "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984)
DA	Ishimoto, S. et al., "A 256K Dual Port Memory," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985)

EXAMINER Glenn Aune	DATE CONSIDERED 3/22/2001
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
AA	4,979,145	12/18/90	Remington et al.	—	—	
GA	5,276,846	01/04/94	Aichelmann Jr., et. al	—	—	

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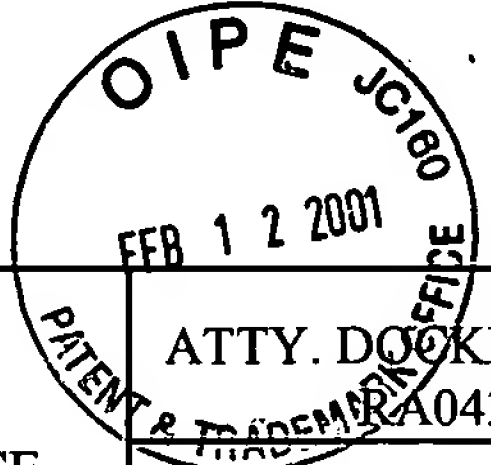
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GA	Tomoji Takada et al., "A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)
GA	Amitai, Z., "Burst Mode Memories Improve Cache Design," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990)
GA	Robert J. Lodi et al., "MNOS-BORAM Memory Characteristics," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976)
GA	Dave Bursky, "ADVANCED SELF-TIMED SRAM PARES ACCESS TIME TO 5 NS", Electronic Design, pp. 145-147 (Feb. 22, 1990)

EXAMINER	Glenn Anne	DATE CONSIDERED	3/22/2001
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
BA	4,482,999	11/13/84	Janson et al.	—	—	
BA	5,029,124	07/02/91	Leahy et al.	—	—	
BA	5,193,193	03/09/93	Iyer	—	—	
BA	4,926,385	05/15/90	Fujishima et al.	—	—	
BA	4,566,099	01/21/86	Magerl	—	—	
BA	4,803,621	02/07/89	Kelly	—	—	
BA	4,589,108	05/13/86	Billy	—	—	
BA	4,870,622	09/26/89	Aria et al.	—	—	
BA	4,878,166	10/31/89	Johnson et al.	—	—	
BA	4,849,965	07/18/89	Chomel et al.	—	—	
BA	4,851,990	07/25/89	Johnson et al.	—	—	

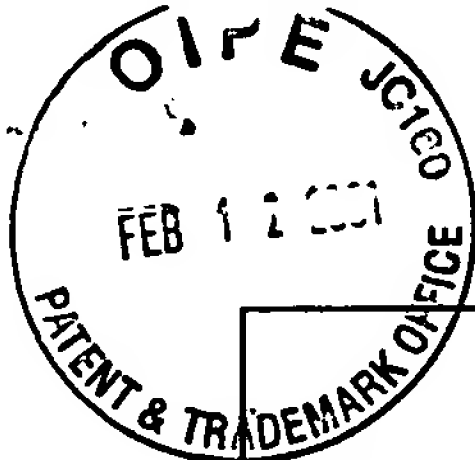
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EXAMINER <i>Glenn Aime</i>	DATE CONSIDERED <i>3/22/2001</i>
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	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE September 25, 2000	GROUP ART UNIT 2181

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
DA	4,528,661	07/09/85	Bahr et al.	—	—	
DA	4,048,673	09/13/77	Hendrie et al.	—	—	
MA	4,748,617	05/31/88	Drewlo	—	—	
MA	4,839,801	06/13/89	Nicely et al.	—	—	
DA	4,949,301	08/14/90	Joshi et al.	—	—	
DA	3,950,735	04/13/76	Patel	—	—	
DA	4,047,246	09/06/77	Kerllenevich et al.	—	—	
DA	4,763,249	08/09/88	Bomba et al.	—	—	
DA	4,625,307	11/25/86	Tulpule et al.	—	—	

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